

APPENDIX



Patent
Serial No. 10/044,091
Agilent Docket No. 10011023-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : SECATCH, Stacey et al.)
Serial No. 10/044,091) Group Art Unit: 2182
Filed: January 10, 2002) Examiner: NGUYEN, Tanh Q.
For: "A NON-DESTRUCTIVE READ FIFO"

STATEMENT ESTABLISHING DILIGENCE

Mail Stop FEE AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

March 25, 2004

Sir:

This is a statement establishing that the Applicants were diligent in filing this application after conceiving of the invention claimed in this application.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop FEE AMENDMENT, Commissioner of Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on the date indicated below.

CMcGrew
Carissa McGrew

APRIL 1, 2004
Date

Claims 1-16 of the present application stand rejected under 35 USC §102(e) as being anticipated by Bentz, Publication Number US 2003/0034797 A1 (hereinafter "Bentz"). Bentz has an effective filing date of August 20, 2001. As indicated on the affidavit being filed herewith under 37 CFR § 1.131, the invention disclosed and claimed in the present application was invented prior to the effective filing date of Bentz. Furthermore, as described below, the Applicants exercised due diligence from a time prior to the effective filing date of Bentz up to the filing of the present application.

Attached is an Agilent Technologies invention disclosure document that describes the invention claimed in the present application. The invention disclosure document was filled out and dated by the inventors, Stacey Secatch and Thomas Henkel. The execution date on the invention disclosure document is June 22, 2001, which is earlier than the effective filing date of Bentz. The execution of the invention disclosure by the inventors was witnessed by Dennis Batchelor, who also executed the invention disclosure document on June 22, 2001.

The Applicants respectfully submit that the executed invention disclosure document is proof that the Applicants conceived the invention prior to the effective filing date of Bentz. In addition, the Applicants exercised due diligence from a time prior to the effective filing date of Bentz up to the filing of the present application.

The filing date of the present application is January 10, 2002, which is less than seven months from the execution date of the invention disclosure document, June 22, 2001. During this time period, the following occurred:

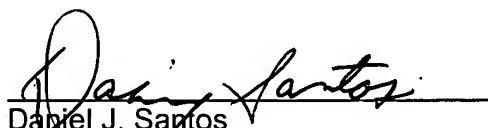
- (1) the invention disclosure document, which includes a detailed textual description of the invention and drawings, was prepared and executed by the inventors;
- (2) the executed invention disclosure document was forwarded by the inventors to the legal department of Agilent Technologies;
- (3) the invention disclosure document was reviewed and processed by the Agilent legal department and forwarded to the undersigned attorney's previous law firm to have the patent application drafted;

(4) the invention disclosure document was reviewed by the undersigned attorney and meetings to discuss the invention were conducted between the undersigned attorney of record and one of the inventors, Stacey Secatch; and

(5) the application was drafted by the undersigned attorney of record and filed in the U.S.P.T.O.

The Applicants respectfully submit that these activities and the short period of time between the preparation and execution of the invention disclosure document and the preparation and filing of the application in the U.S.P.T.O. clearly show that due diligence was exercised from a time prior to the effective filing date of Bentz to the filing of the present application in the U.S.P.T.O.

Respectfully submitted,
GARDNER GROFF, P.C.


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INVENTION DISCLOSURE

COPY

PAGE ONE OF 3

PDNO 10011023 DATE RCVD 6/27/01

ATTORNEY FEA

CIC-FCS

Instructions: The information contained in this document is **COMPANY CONFIDENTIAL** and may not be disclosed to others without prior authorization. Submit this disclosure to the Agilent Technologies Legal Department as soon as possible. No patent protection is possible until a patent application is authorized, prepared, and submitted to the Government.

Descriptive Title of Invention:

Non-destructive read FIFO

Name of Project:

Tonic

Product Name or Number:

2AS3

Was a description of the invention published, or are you planning to publish? If so, the date(s) and publication(s):

No

Was a product including the invention announced, offered for sale, sold, or is such activity proposed? If so, the date(s) and location(s):

No

Was the invention disclosed to anyone outside of AGILENT TECHNOLOGIES, or will such disclosure occur? If so, the date(s) and name(s):

No

If any of the above situations will occur within 3 months, call your IP attorney or the Legal Department now at 1-553-3061 or 408-553-3061.

Was the invention described in a lab book or other record? If so, please identify (lab book #, etc.)

No

Was the invention built or tested? If so, the date:

No

Was this invention made under a government contract? If so, the agency and contract number:

No

Description of Invention: Please preserve all records of the invention and attach additional pages for the following. Each additional page should be signed and dated by the inventor(s) and witness(es).

- A. Prior solutions and their disadvantages (if available, attach copies of product literature, technical articles, patents, etc.).
- B. Problems solved by the invention.
- C. Advantages of the invention over what has been done before.
- D. Description of the construction and operation of the invention (include appropriate schematic, block, & timing diagrams; drawings; samples; graphs; flowcharts; computer listings; test results; etc.)

Signature of Inventor(s): I (we) hereby submit this disclosure on this date:

311658 Stacy Secatch

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(If more than four inventors, include additional information on another copy of this form and attach to this document)



Signature of Witness(es): (Please try to obtain the signature of the person(s) to whom invention was first disclosed.)

The invention was first explained to, and understood by, me (us) on this date: []

Full Name

DENNIS B BATCHELOR

Signature

Dennis B Batchelor

Date of Signature

6-22-01

Full Name

Signature

Date of Signature

Inventor & Home Address Information: (If more than four inventors, include addl. information on a copy of this form & attach to this document)

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Stacey Seratch 6/22/2001

Prior solution

FIFOs are a standard implementation of a queue, where one can load in data in a sequence, and unload the same data in the same sequence. There are also informational signals empty, indicating that there is no valid data in the queue, and full, the queue can no longer be written as there is no room.

RAMs (random access memory) allow a write and read to any location in the fifo, but the operation is often more complex. Many can not do both a read and write in the same state. They generally have higher latency setting up address changes to data being written/being read. For small memory sizes, they are often generally larger than FIFOs as well.

One major construct in code is a 'for' loop, where the same code is executed many times in sequence. If the first pass of the loop could be cached, follow-loops could be executed from the memory. A FIFO will not work because the stream is linear. A RAM will work, but from above will generally be slower and larger for small caches.

B. Problems solved

A non-destructive read FIFO will allow the data to be written linearly as well as read linearly, but allows multiple reads. It can now behave as a cache for the initial instructions in the loop up to the size of the cache.

C. Advantages

Because the instructions will not need to be fetched from memory, throughput to external memory is decreased along with latency to the first instruction in the loop because it is available immediately on chip.

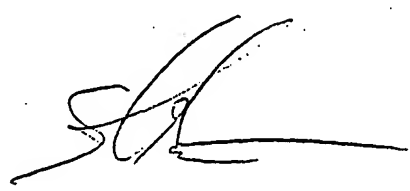
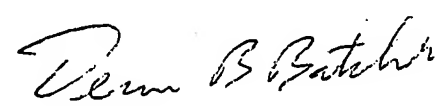
D. Description

There are two pointers in the FIFO, a write pointer and a read pointer. Both can be reset independantly. A write will occur while in 'loop-mode', 'first' is active and there is room in the fifo. A read will occur when in 'loop-mode', 'first' is non-active, and there is data in the fifo.

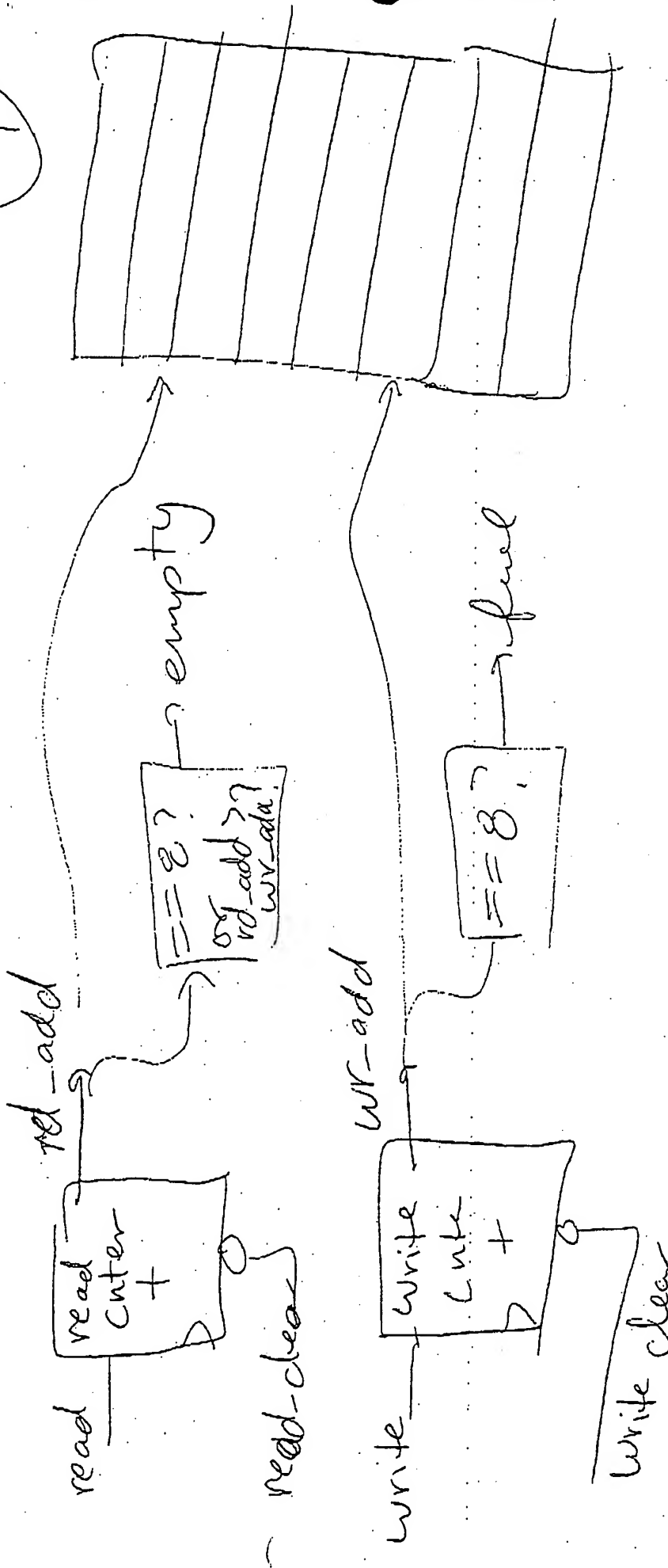
A loop in the architecture has the construct:
set the counter to the number of loops to execute
jump to subroutine, set return to pc - 1 if counter 0, pc if non-zero; dec counter
execute subroutine, until return encountered, then jump to return value.
After loop is completed, the instruction after the jump to sub is executed.

When the counter is set and a jump is detected, 'loop-mode' and 'first' are set. This will also clear out the write pointer. Therefore the first execution of the loop is stored. The return will automatically set 'first' low. However, 'loop-mode' will stay high until the final return of the loop. Upon the next jump to subroutine, the read pointer will be clear out. With 'first' low and 'loop-mode' set, all of the following iterations can be read from the FIFO.

Finally, this architecture has a fixed level of subroutines. Therefore, each level of subroutine can have it's own loop FIFO. As a consequence, multiple levels of loops can all be executed and stored into their own FIFOs.

 6/22/2001  6-22-01

4



btw, the ~~pushback~~ pushback fto structure is also available for the "main" loop. Since we return to current add, or current add + 1, chances are that we will use the data we have fetched but haven't yet executed.

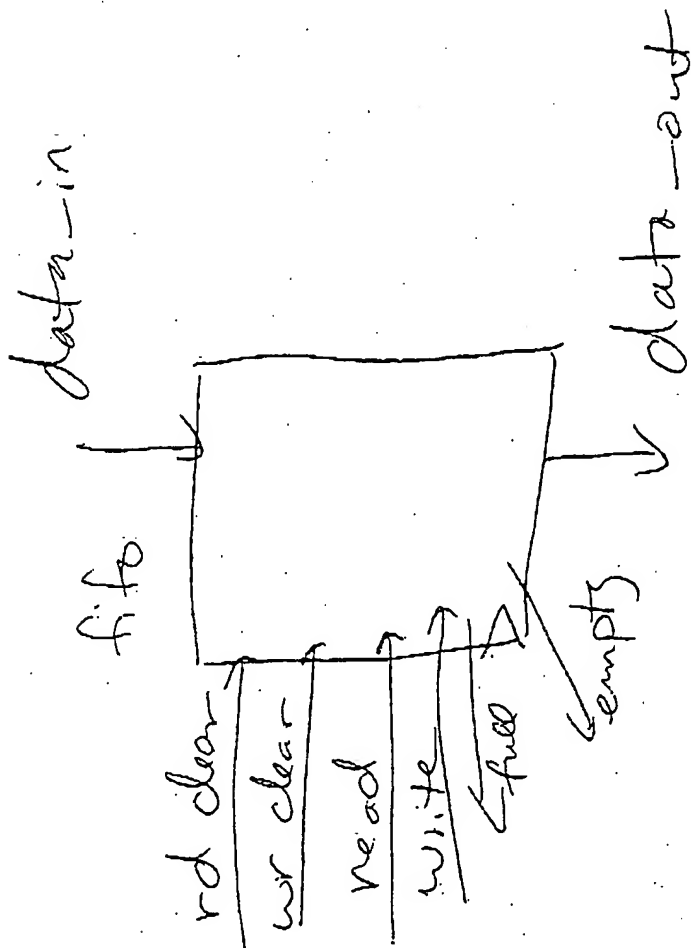
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Subsequent
passes read is
Set for each

inst ... ,

empty when @

read, or when
move read then
written



first IMPC after RPT fires
rd-clear/wr-clear

for first Pass write
is Set ...

internal address
increments
Full when all 8
addresses written

RPT n
JMPC subtag
INST 0

says execute
subtag loop
n times

(1)

subtag: INST 1
INST 2
INST 3
INST 4
INST 5
INST 6
INST 7
INST 8
INST 9
INST 10

contains a return
statement

first pass

RPT n
JMPC subtag

says next inst will be
repeated

push back used here
to save into
a "return fifo"

long time for
initial fetch
from mem

INST 1

saved
into
cache

data in the
sublevel marked
invalid

INST 8

INST 9

INST 10

lets not 95/1/20 available from storage
~~lets not 95/1/20 available from storage~~
INST 10 } from main
INST 9 }
INST 8 }
INST 1 } from cache
IMPC subtag ← allowed to load from storage

INST 10 } from main
INST 9 }
INST 8 }
INST 1 } from cache
IMPC subtag
INST 10
INST 9
} some time?

INST 8
} immediately from cache
available
INST 1 }
lets INST 9

IMPC subtag ← push back again

①